A NOVEL CONTRIBUTION TO THE RTD-BASED THRESHOLD LOGIC FAMILY[1]

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ABSTRACT

Many logic circuit applications of Resonant Tunneling Diodes are based on the MOnostable-BIstable Logic Element (MOBILE). Threshold logic is a computational model widely used in the design of MOBILE circuits, i.e. these circuits are built from threshold gates. More recently, generalized threshold gates, also suitable to be realized with MOBILE RTD structures, are being investigated. In this paper we propose a novel MOBILE circuit topology obtained by exploiting threshold logic concepts and properties. A comparison in terms of speed and power performance between the proposed topologies and previous reported ones is carried out.

Index Terms **-RTDs, MOBILE, Threshold Logic**

I. INTRODUCTION

Resonant tunnelling diodes (RTDs) are very fast non linear circuit elements which exhibit a negative differential resistance (NDR) region in their current-voltage characteristics (Figure 1a) which can be exploited to significantly increase the functionality implemented by a single gate. Circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE). The MOBILE [1] (Figure1a) is a rising edge triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage (V_{bias}). When V_{bias} is low, both RTDs are in the on-state (or low resistance state) and the circuit is monostable. Increasing V_{bias} to an appropriate maximum value ensures that only the device with the lowest peak current switches (*quenches*) from the on-state to the off-state (the high resistance state). Output is high if the driver RTD is the one which switches and it is low if the load switches. Assuming equal current densities for both RTDs, peak currents are proportional to RTD areas λ_1 and λ_2 for load and driver respectively. When $\lambda_1 < \lambda_2$ the load switches (the output V_{out} goes to low or "0") and if otherwise when $\lambda_2 < \lambda_1$ the driver switches (the output V_{out} goes to high or "1"). Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. In the configuration for an inverter MOBILE shown in Figure1b, the peak current of the driver RTD can be modulated using the external input signal V_{in}. During a critical period when V_{bias} rises, the voltage at the output node V_{out} goes to one of the two stable states (low or high), corresponding to "0" and "1" in binary logic. RTD areas are selected such that the value of the output depends on whether the external input signal V_{in} is "1" or "0". For $V_{bias} = 1$ the output node maintains its value even if the input changes. That is, this circuit structure is self-latching allowing to implement pipeline at the gate level without any area overhead associated to the addition of the latches which allows very high throughoutput.

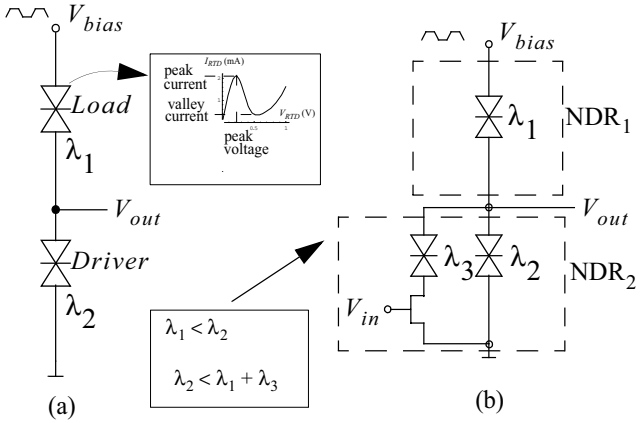

Figure 1.-a) Basic MOBILE, (b) MOBILE inverter.

This circuit topology has been extended to systematically implement threshold gates. Figure 2a shows the RTD/HFET implementation of a generic threshold gate [2] defined as $V_{out} = 1$ *iff* $w_1x_1 + w_2x_2 - w_3x_3 - w_4x_4 \geq T$, and 0 otherwise. The RTD areas determine the weights w_i, $(i = 1, \ldots, 4)$ and the threshold *T*. Input stages controlled by external inputs are placed in parallel to RTD$_1$ or RTD$_2$ depending on whether the associated weight is positive or negative, allowing the control of the peak currents of both NDRs.

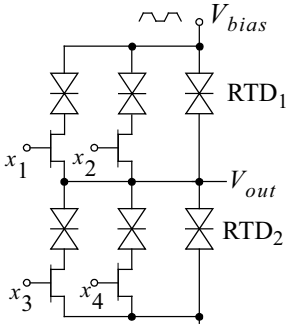

Figure 2.-Generic MOBILE TG .

More recently, generalized threshold gates, also suitable to be realized with MOBILE RTD structures, are being investigated [3], [4], [5]. In this paper we propose a novel MOBILE topology obtained by exploiting threshold logic concepts and properties.

II. LOGIC MODEL SUPPORTING THE NEW GATE

For the sake of clarity, let us consider a two-input function, the EXOR, $f(x_2, x_1) = x_1 \oplus x_2$, to illustrate the relationship between generalized threshold logic and MOBILE circuit topologies, as well as to introduce the proposed topology. This function is not a threshold function however, a number of MOBILE implementations are possible if we generalize the threshold logic concepts.

Figure 3 depicts its realization as a Multi-Threshold Threshold Gate (MTTG) [3]. Multi-threshold threshold gates (MTTGs) are a generalization of the conventional TGs in which there are k thresholds, T_1,...T_K, rather than the usual single threshold, T. $K + 1$ RTDs connected are required instead of the two of the basic MOBILE. The output of a two-input two-threshold MTTG is 1 for $T_1 \le w_1x_1 + w_2x_2 < T_2$ and 0 for $w_1x_1 + w_2x_2 < T_1$ and $T_2 \le w_1x_1 + w_2x_2$. Clearly, for $w_1 = w_2 = 1$, $T_1 = 1$, and $T_2 = 2$, this corresponds to the EXOR function.

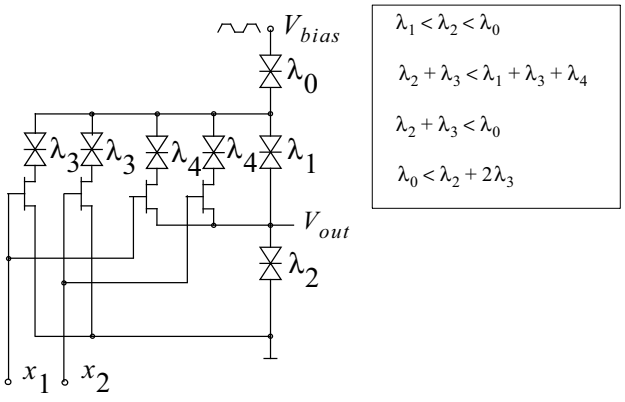

Figure 3.-2-input EXOR realized as an MTTG.

Figure 4 depicts a realization reported in [4] and which can be explained as a TG over an extended input set (GTG1). The EXOR is realized as the TG with the extended set of input variables, $\{y_1, y_2, y_3\}$, given by $\{x_1, x_2, x_1 \wedge x_2\}$, $w_1 = w_2 = 1$, $w_3 = -2$, and threshold at 1.

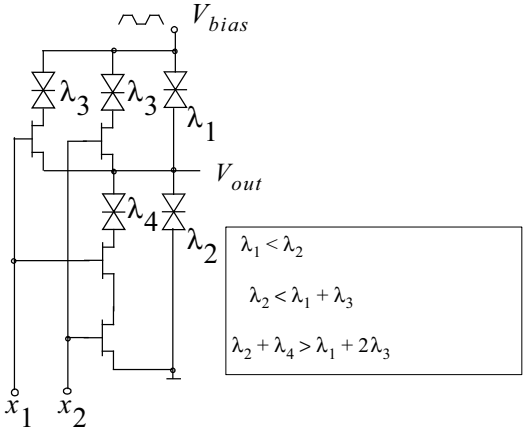

Figure 4.-2-input EXOR from [4] (GTG1).

Figure 5 shows a realization using the logic style proposed in [5] (GTG2). This realization is obtained since the 2-input EXOR can be explained as a a TG over the extended set of input variables given by $\{x_1 \vee x_2, x_1 \wedge x_2\}$, $w_1 = 2$, $w_2 = -2$ and threshold at 1. Note that the two upper input branches in Figure 4 have been combined.

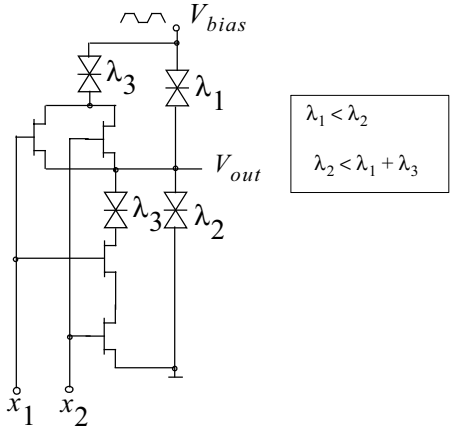

Figure 5.-2-input EXOR from [5] (GTG2)

From the performance point of view, MOBILE TGs with only negative weights (all input branches in parallel with driver RTD) are superior since transistors associated to positive weights are larger to compensate reduced gate to source voltages, which increases capacitances. Thus, it would be desirable to obtain representations for the target functions with only negative weights. In addition, having all branches in parallel could

enable additional combinations. We are able to obtain such a representation by applying a basic property of threshold functions which states that given a threshold function $f(x_n...x_1)$, with weights w_i, $1 \le i \le n$, and threshold T, the function $f(x_n...\bar{x}_j...x_1)$ is also a threshold function with weights $w'_i = w_i$, $i \neq j$, $w'_j = -w_j$ and $T' = T - w_j$. For our EXOR example, this means that it can be represented as a TG over the set of input variables, $\{y_1, y_2\}$, given by $\{\overline{x_1 \vee x_2}, x_1 \wedge x_2\}$, $w_1 = w_2 = -2$ and threshold at -1. In addition, it can be described as a TG with a single input variable, given by $\{y_1\}$, $\{\overline{(x_1 \vee x_2)} \vee (x_1 \wedge x_2)\}$, $w_1 = -2$ and threshold at -1. Figure 6 depicts the circuit realization obtained from this model (GTG3). Note that areas of driver and load RTDs are interchanged with respect to GTG2 and that two inverters are required. Pipelined operation of cascaded GTG3 (with the inverters which do not exist in any previously reported MOBILE topology) has been validated through extensive simulations of several complex examples.

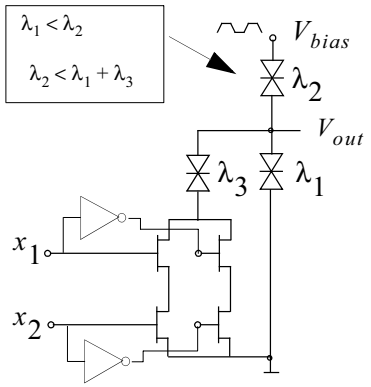

Figure 6.-Proposed 2-input EXOR (GTG3).

III. COMPARISON OF TOPOLOGIES

Two-input EXOR gates have been designed with the different described topologies using the same technology. Transistors and RTDs have been sized to optimize operating frequency in each topology. Table I summarizes performance in terms of frequency and power-delay product obtained through simulation of three stage chains of gates using models based on InP RTDs and HFETS. Inverters required by the topology proposed in this paper have been included in the simulations. Table II depicts results for a more complex function: $f(x_4, x_3, x_2, x_1) = x_1x_2 \oplus x_3x_4$. This function has been selected since it is the one used in [5] to illustrate the logic style described in that paper. MTTG realization has not been

Table I: Simulation results for 2-input exor. PDP = (P@F_{max})/F_{max}

Style	F_{max} (GHz)	$PDP/PDP_{proposed}$
MTTG	1.75	3.25
GTG1	0.83	5.5
GTG2	1.14	3.25
GTG3 (including inverters)	4	1

Table II: Simulation results for $f(x_4, x_3, x_2, x_1) = x_1x_2 \oplus x_3x_4$

Style	Fmax (GHz)	$PDP/PDP_{proposed}$
GTG2	0.53	2
GTG3 (including inverters)	1.47	1

considered since it is not practical for this example. It is a four-threshold threshold function which would require five series-connected RTDs. Advantages of the novel realizations proposed are clearly observed. Better speed and PDP are exhibited by the proposed circuits, in spite of requiring the inverters which consumes power.

For more complex examples, the proposed GTG3 topology is not unique. That is, a set of solutions exhibiting different power-speed tradeoffs. For example, the function $f(x_7, x_6, x_5, x_4, x_3, x_2, x_1) = x_1x_2 + x_3x_4 + x_5x_6 + x_7$ can be clearly represented as a generalized TG on the set of inputs $\{y_1, y_2, y_3, y_4\}$, given by $\{x_1 \wedge x_2, x_3 \wedge x_4, x_5 \wedge x_6, x_7\}$, $w_1 = w_2 = w_3 = w_4 = 1$ and threshold at 1. Different GTG3 realizations are possible. Let us describe two of them which will be denoted as GTG3a and GTG3b. Realization GTG3a is obtained as a generalized TG with input variable $\{y_1\} = \{\overline{(x_1 \wedge x_2) \vee (x_3 \wedge x_4) \vee (x_5 \wedge x_6) \vee x_7}\} = \{(\overline{x_1} \vee \overline{x_2}) \wedge (\overline{x_3} \vee \overline{x_4}) \wedge (\overline{x_5} \vee \overline{x_6}) \wedge \overline{x_7}\}$, with a weight $w_1 = -1$ and $T = 0$. It corresponds to having combined the four branches in GTG1, and moving the resulting one from load to driver apliying the transformation property in Section 2. GTG3b is obtained as a generalized TG with the set of input $\{y_1, y_2, y_3, y_4\} = \{\overline{x_1 \wedge x_2}, \overline{x_3 \wedge x_4}, \overline{x_5 \wedge x_6}, \overline{x_7}\}$ weights $w_1 = w_2 = w_3 = w_4 = -1$ and $T = -3$. The four

branches in GTG1 are moved now without combining them. Figure 7 depicts both topologies GTG3a and GTG3b. Table III summarizes performance in terms of frequency and power delay product, it is important to realize that the GTG3b topology shows a better performance in terms of frequency due to the fact of that this topology has not a large serie-connection of transistors. However the GTG3a topology has a better power delay product due to the fact that in this topology less number of devices are required and therefore less power consumption than GTG3b topology.

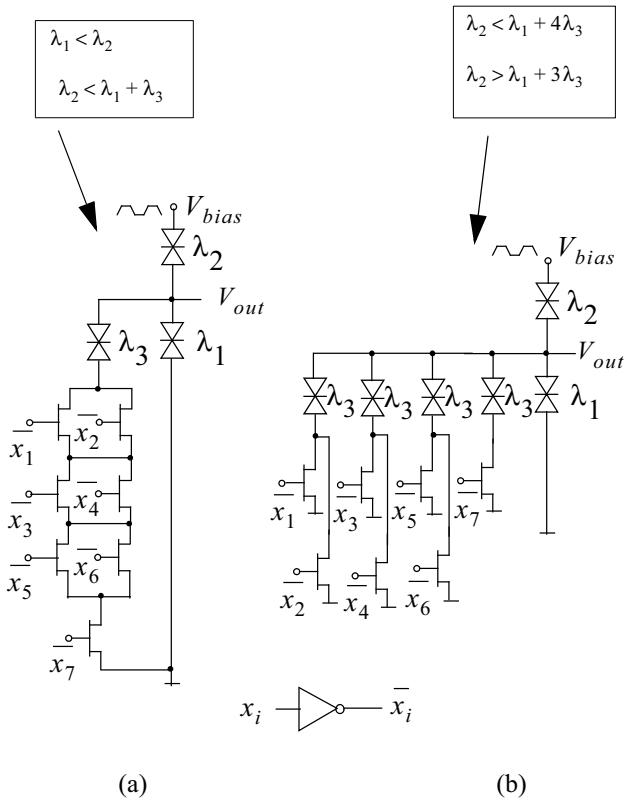

Figure 7.- Topologies for function $x_1x_2 + x_3x_4 + x_5x_6 + x_7$, (a) GTG3a and (b) GTG3b.

Table III: Simulation results for the function depicted in the Figure 7

Style	Fmax (GHz)	PDP_{GTG3}/PDP_{GTG4}
GTG3a	0.77	0.91
GTG3b	1.23	1

IV. CONCLUSION

Additional comments are in order to clarify characteristics of each logic style that might be hidden by the chosen examples. The computational model supporting the GTG1 topology can be systematically obtained through a transformation matrix from the description of the target function in the boolean domain [4]. GTG1 is a TG in the input set formed by positive literals of the input variables and logic products of positive literals of input variables. The GTG2 topology is not restricted to single input branches in parallel with driver and load RTDs. It has been reported [5] that any 4-input function can be realized with a maximum of four input branches (two in parallel with the driver and two in parallel with the load). GTG2 is a TG in an input set formed by arbitrary functions of positive literals of input variables. There are not input branches in parallel with load RTD in GTG3. It is a TG in the input set formed by arbitrary sums of products (products of sums) of both positive and negative literals. This is one of the main differences with the MOBILE gates in [6] with a single input branch composed of a transistor network driven by positive literals. GTG3 is more flexible. Negative literals eliminate restrictions in the functionality that can be implemented and the use of more than one input branch can reduce the complexity of the required transistor network allowing different power-speed trade-off.

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